ABSTRACT OF THE DISCLOSURE

A body diode comparator circuit for a synchronous rectified FET driver including a sample circuit and a comparator. The FET driver has a phase node coupled between a pair of upper and lower switching FETs and is responsive to a PWM signal having first and second phases for each cycle. The sample circuit samples an initial voltage of the phase node during the first phase of the PWM signal and provides a sum voltage indicative of the initial phase voltage added to the voltage level of the phase node during the second phase of the PWM signal. The comparator compares the sum voltage with a predetermined reference voltage and provides an output indicative of an activation state of the lower FET during the second phase of the PWM signal. The FET driver turns on the upper FET when the comparator indicates that the lower FET is off.